

Ver 1.2

**Radiation Hardened 5V Quad
Differential Line Receiver**

Datasheet

Part Number: B26C32CERH



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Page of Revise Control

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1. Features

- Single 5V Supply
- CMOS Compatible Outputs
- High Impedance Outputs when Disabled or Powered Down
- EIA RS-422 Compatible Inputs
- Full -55°C to +125°C Military Temperature Range
- Radiation-hardened design:
 - Total-dose: 100 krad(Si)
 - Latchup immune ($LET > 75\text{MeV}\cdot\text{cm}^2/\text{mg}$)
- Packaging options:
 - 16-lead Flatpack
 - 16-lead Dual-In-Line Package
- Low quiescent current
- Input Fail Safe Circuitry

2. General Description

The B26C32CERH is a quad differential line receiver designed for digital data transmission over balanced lines and meets the requirements of EIA Standard RS-422. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

3. Function Block Diagram

B26C32CERH function block diagram is shown in figure 3-1.

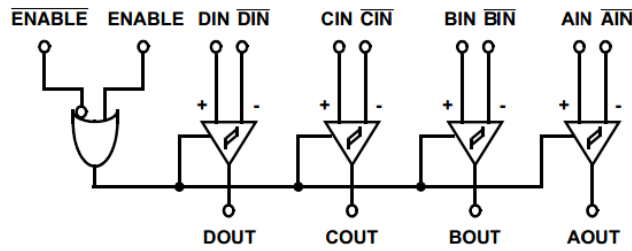


Figure 3-1 B26C32CERH function block digram

4. Packages and Pin Function Descriptions

The provided package is: FP16 and DIP16.

B26C32CERH-pin configuration is shown in 4-1.

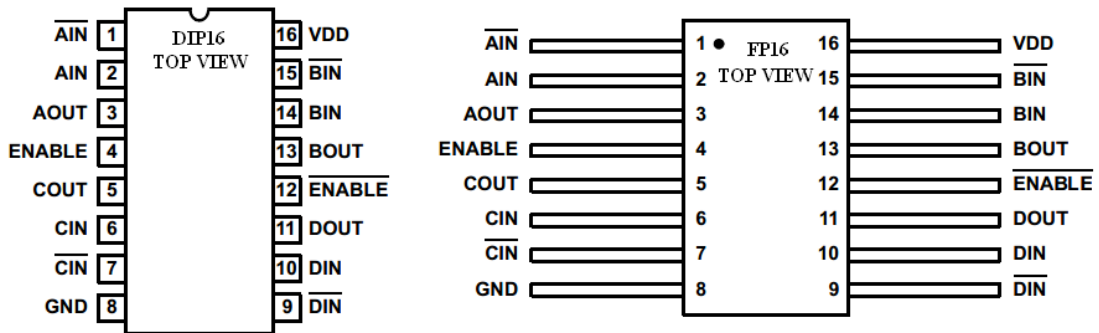


Figure 4-1 B26C32CERH pin configuration

Table 4-1 B26C32CERH Pin Function Descriptions

Pin No.	Name	Description
1, 7, 9, 15	\overline{AIN} , \overline{CIN} , \overline{DIN} , \overline{BIN}	Inverting receiver input pin
2, 6, 10, 14	AIN,CIN,DIN,BIN	Non-inverting receiver input pin
3, 5, 11, 13	AOUT,COUT,DOUT,BOUT	Receiver output pin
4	ENABLE	Active high enable pin
12	\overline{ENABLE}	Active low enable pin
16	VDD	Power supply pin
8	GND	Ground pin

5. Pin List

B26C32CERH- pin list is shown in table 5-1.

Table 5-1 B26C32CERH- pin list

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	\overline{AIN}	INPUT DATA1 NEGATIVE	9	\overline{DIN}	INPUT DATA4 NEGATIVE
2	AIN	INPUT DATA1 POSITIVE	10	DIN	INPUT DATA4 POSITIVE
3	AOUT	OUTPUT DATA1	11	DOUT	OUTPUT DATA1
4	ENABLE	Active high enable pin	12	\overline{ENABLE}	Active low enable pin
5	COUT	OUTPUT DATA3	13	BOUT	OUTPUT DATA2
6	CIN	INPUT DATA3 POSITIVE	14	BIN	INPUT DATA2 POSITIVE
7	\overline{CIN}	INPUT DATA3 NEGATIVE	15	\overline{BIN}	INPUT DATA2 NEGATIVE
8	GND	GND	16	VDD	POWER

6. Detailed Description

6.1 Function Description

The B26C32CERH can detect signals as low as $\pm 400\text{mV}$ over the common mode range of -7V to $+7\text{V}$. The receivers are also equipped with input fail safe circuitry, which causes the outputs to go to a logic “1” when the inputs are open. Enable and Disable functions are common to all four receivers. truth table is shown in table 6-1.

Table 6-1 truth table

ENABLE	\overline{ENABLE}	Input	Output
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq V_{Th} (\text{Max})$	H
		$V_{ID} \leq V_{Th} (\text{Min})$	L
		Open	H

L = Low logic state
X = Irrelevant
H = High logic state
Z = TRI-STATE (high impedance)

6.2 Storage Condition

Packaged product should be stored in the ventilate warehouse with ambient temperature $10^{\circ}\text{C}\sim 30^{\circ}\text{C}$ and relative humidity less than 70%. There should be no acid, alkali or other radiant gas in the environment,

6.3 Absolute Maximum Ratings

- a) Supply voltage (V_{DD}) : $-0.5\text{ V}\sim 7.0\text{ V}$
- b) Common Mode Range (V_{CM}): $\pm 12\text{ V}$
- c) Differential Input Voltage (V_{Diff}): $\pm 12\text{ V}$
- d) Enable Input Voltage (V_I): $-0.5\text{ V}\sim V_{DD} + 0.5\text{ V}$
- e) Storage temperature (T_{stg}) : $-65^{\circ}\text{C}\sim 150^{\circ}\text{C}$
- f) Lead temperature (T_h) : 260°C

6.4 Recommended Operation Conditions

- a) Supply Voltage (V_{DD}): $4.5\text{ V}\sim 5.5\text{ V}$
- b) Common mode range (V_{CM}) : $\pm 7\text{ V}$
- c) Input low voltage (V_{IL}) : $0\sim 0.3V_{DD}\text{ max}$
- d) Input high voltage (V_{IH}) : $V_{DD}\sim 0.7V_{DD}\text{ min}$
- e) Input rise and fall time (t_{IT}) : 500 ns max
- f) Case operation temperature range(TA) : $-55^{\circ}\text{C}\sim 125^{\circ}\text{C}$

7. Specifications

All electrical characteristics are shown in table 7-1, Propagation Delay and Transition Time Waveforms are shown in Figure 7-1, Three-State Delay Waveform is shown in Figure 7-2.

Table 7-1 B26C32CERH electrical characteristics

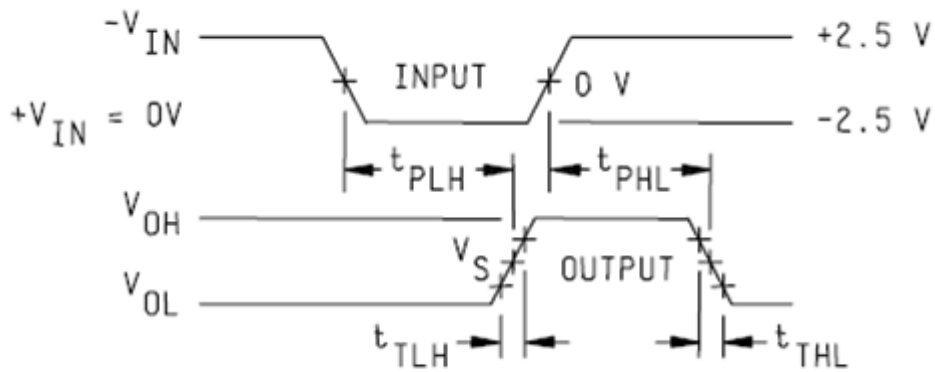
PARAMETER	SYMB OL	CONDITION ($-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, $V_{DD}=5.0 \times (1 \pm 10\%) \text{ V}$) unless otherwise specified	LIMIT		UNIT
			MIN	MAX	
Enabled high level input voltage	V_{IH}	$V_{DD}=4.5\text{V}, 5.5\text{V}$	0.7* V_{DD}	—	V
Enabled low level input voltage	V_{IL}	$V_{DD}=4.5\text{V}, 5.5\text{V}$	—	0.3* V_{DD}	V
High-level output voltage	V_{OH}	$V_{DD}=4.5\text{V}, V_{DIFF}=1.0\text{V}, I_O = -6\text{mA}$	4.1	—	V
Low-level output voltage	V_{OL}	$V_{DD}=4.5\text{V}, V_{DIFF}=-1.0\text{V}, I_O = 6\text{mA}$	—	0.4	V
Input leakage current, enable pins	I_{IN}	$V_{IN}=0\text{V}, 5.5\text{V}, V_{DD}=5.5\text{V}$	-1.0	1.0	μA
Differential input voltage	V_{TH}	$V_{DD}=4.5\text{V}, -7\text{V} < V_{CM} < 7\text{V}$	-0.4	+0.4	V
Input current high (differential inputs)	I_{INH}	$V_{DD}=5.5\text{V}, +V=10\text{V}, -V=0\text{V}$ And $+V=0\text{V}, -V=10\text{V}$	—	1.8	mA
Input current low (differential inputs)	I_{INL}	$V_{DD}=5.5\text{V}, +V=-10\text{V}, -V=0\text{V}$ And $+V=0\text{V}, -V=-10\text{V}$	-2.7	—	mA
Output Three-State Current	I_{OZ}	$V_{DD}=5.5\text{V}, \text{ENABLE}=0\text{V}, \overline{\text{ENABLE}}=5.5\text{V}, V_o=V_{DD} \text{ or } \text{GND}$	-5.0	5.0	μA
Standby supply current	I_{DDSB}	$V_{DD}=5.5\text{V}, V_{DIFF}=1.0\text{V},$ Outputs= open	—	25	mA
Input clamp voltage	V_{IC}	$I_{IC} = -1 \text{ mA}$	-1.5	—	V
		$I_{IC} = 1 \text{ mA}$	—	1.5	V
Input hysteresis ^a	V_{HYST}		20	100	mV
Input resistance	R_{IN}	$-7\text{V} \leq V_{CM} \leq 7\text{V}$	4	20	k Ω
Function test	FT	$f = 10\text{MHz}$			
Fail safe	F_{SAFE}	+ and – inputs are open, $V_{OUT} = \text{logic "1"}$	4.1	—	V
Differential Propagation Delay High to Low	t_{PHL}	$V_{DD}=4.5\text{V}, V_{DIFF}=2.5\text{V}$ Figure 7-1	6	40	ns
Differential Propagation Delay Low to High	t_{PLH}	$V_{DD}=4.5\text{V}, V_{DIFF}=2.5\text{V}$ Figure 7-1	6	40	ns

Rise Time	t_{TLH}	$V_{DD}=4.5V, V_{DIFF}=2.5V$ Figure 7-1	2	12	ns
Fall Time	t_{THL}	$V_{DD}=4.5V, V_{DIFF}=2.5V$ Figure 7-1	2	12	ns
Disable Time High to Z	t_{PHZ}	$V_{DD}=4.5V, V_{DIFF}=2.5V$ Figure 7-2	6	29	ns
Disable Time Low to Z	t_{PLZ}	$V_{DD}=4.5V, V_{DIFF}=2.5V$ Figure 7-2	6	29	ns
Enable Time Z to High	t_{PZH}	$V_{DD}=4.5V, V_{DIFF}=2.5V$ Figure 7-2	3	18	ns
Enable Time Z to Low	t_{PZL}	$V_{DD}=4.5V, V_{DIFF}=2.5V$ Figure 7-2	3	18	ns
Input capacitance ^a	C_{IN}	$V_{DD} = \text{open}, f = 1 \text{ MHz}$	—	12	pF
Output capacitance ^a	C_{OUT}	$V_{DD} = \text{open}, f = 1 \text{ MHz}$	—	12	pF

Notes:

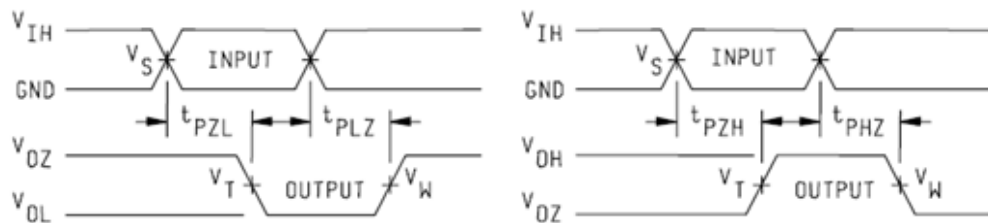
- 1、 Devices are tested @ $V_{DD} = 4.5V \& 5.5V$.
- 2、 Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages.

^a Parameter is guaranteed by design or process, but not tested.



NOTE : $V_{DD}=4.5V$ $GND=0V$ $V_S=50\%$

Figure.7-1. Receiver Propagation Delay and Transition Time Waveforms



NOTE : $V_{DD}=4.5V$ $V_{IH}=4.5V$ $V_S=50\%$ $V_T=50\%$ $V_W=V_{OL}+0.5V$ **NOTE : $V_{DD}=4.5V$ $V_{IH}=4.5V$ $V_S=50\%$ $V_T=50\%$ $V_W=V_{OH}-0.5V$**

Figure.7-2. Receiver Three-State Delay Waveform

8. Package Specifications

B26C32CERHF adopt 16-Lead Ceramic Quad Flat package, as in Figure 8-1 and the size is listed in Table 8-1. B26C32CERHD adopt 16-lead Dual-In-Line Package, as in Figure 8-2 and the size is listed in Table 8-2.

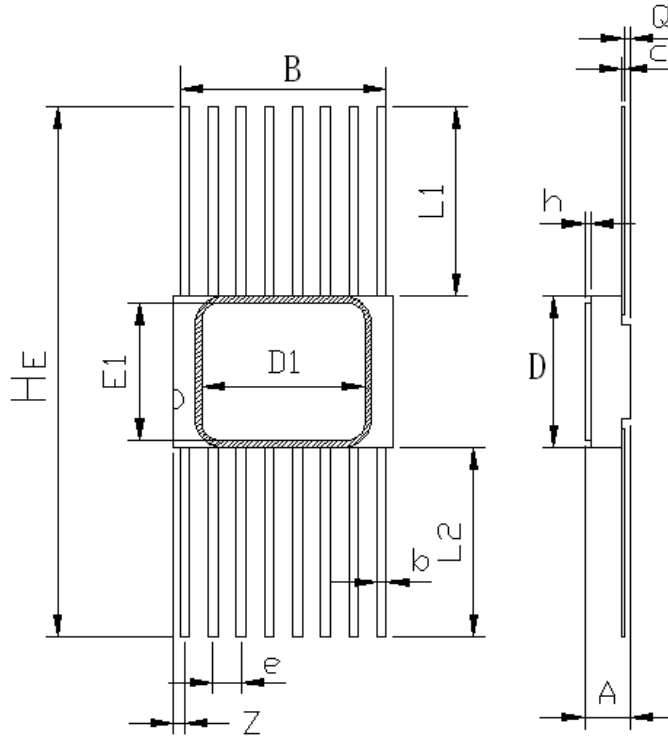


Figure.8-1. Flat Package Outline

Table 8-1 Flat Package Size

Symbol	Value (unit: mm)		
	Min	Normal	Max
A	1.60	—	2.50
B	8.94	—	9.69
b	0.25	—	0.54
c	0.07	—	0.20
D	6.55	—	7.25
e	—	1.27	—

He	18.76	19.41	20.06
Q	0.13	—	0.90
L1	5.75	—	6.75
L2	5.75	—	6.75
Z	—	—	1.27
D1	—	7.366	—
E1	—	6.223	—
h	0.22	—	0.28

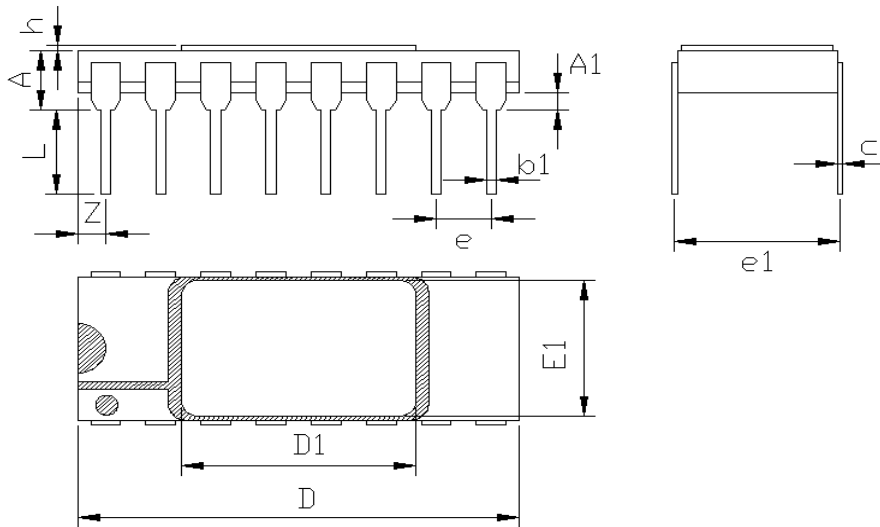


Figure.8-2. Dual-In-Line Package Outline

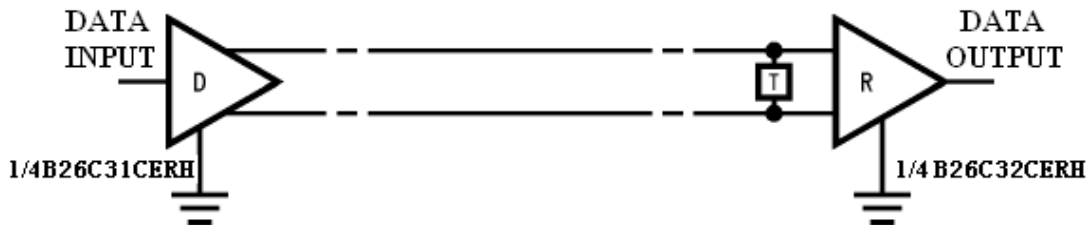
Table 8-2 Dual-In-Line Package Size

Symbol	Value (unit: mm)		
	Min	Normal	Max
D	20.00	—	20.58
D1	—	10.795	—
E1	—	6.985	—
h	0.22	—	0.28

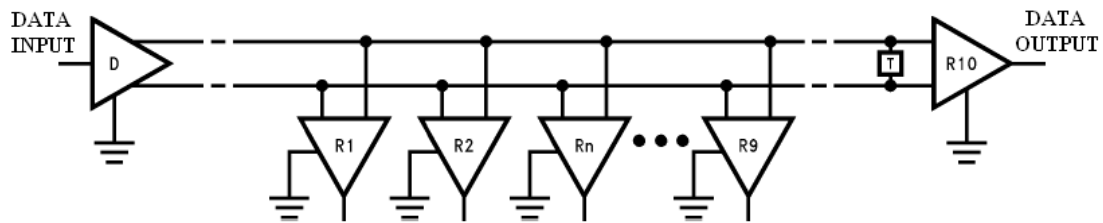
e1	—	7.62	—
e	—	2.54	—
c	0.20	—	0.36
Z	—	—	2.54
A	—	—	5.1
A1	0.51	—	—
b1	0.35	—	0.59
L	2.54	—	5.0

9. Appendix I Typical Application Example

The B26C32CERH receiver's intended use is primarily in an uncomplicated point-to-point configuration as is shown in Appendix figure 1-1. This configuration provides a clean signaling environment for quick edge rates of the drivers. The receiver is connected to the driver through a balanced media such as a standard twisted pair cable. Typically, the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media and is located as close to the receiver input pins as possible. Other configurations are possible such as a multireceiver configuration, Multidrop configuration as is shown in Appendix figure 1-2.



Appendix figure 1-1 Point-to-Point Application



Appendix figure 1-2 Multidrop Application

10. Appendix II Replaced Product

Appendix table1-1

Device Type	Substituted Device Type
B26C32CERHD	HS1-26C32RH-Q
B26C32CERHF	HS9-26C32RH-Q

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