Ver 1.0

A Scrubbing Circuit for Virtex5

Datasheet

Part Number： BM501-003CBRH

北京微电子技术研究所

Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	2018.10		Initial release.	

TABLE OF CONTENTS

1、 Features

- **Scrubbing features**
  - The type of the object FPGA can be identified automatically.
  - It supports power on configuration, blind scrubbing, readback scrubbing and FLASH ECC function.
  - It supports SEFI monitoring and restoration function.
  - It can scrub 1 to 4 FPGA chips at the same time.
  - The configuration and scrub mode is Slave-SelectMAP.
  - Xilinx PROM or NOR Flash are used as bitstream storage chips.
  - The UART interface communication function is available.
  - The bitstream can be reloaded to FLASH in orbit.
- **Electrical characteristics**
  - 3.3V I/O voltage, 1.8V core voltage
  - Operation frequency：20MHz
  - Power consumption：< 500mW
- **Reliability features**
  - Operation temperature ：-55℃ ～ +125℃
  - ESD feature （human body model）：2000V
  - Electrical latch up feature：200mA
  - Total ionizing dose：≥100Krad（Si）
  - Single event latch-up threshold：≥75MeV·cm^2/mg
  - Single event upset threshold：≥37MeV·cm^2/mg

2、 General Description

BSV5CBRH is an ASIC for scrubbing configuration memories in SRAM based FPGAs. BSV5CBRH can support 1 to 4 Xilinx Virtex/Virtex2/Virtex4/Virtex5 serial FPGA chips, including XQVR300, XQR2V3000, XQR4VSX55T, XQR5VSX95T, XQR5VLX155T, XQR5VFX130T, as well as the BMTI fully compatible aerospace grade FPGAs BQVR300RH, BQR2V3000, BQR5VSX95T, BQR5VLX155T. BSV5CBRH has power on configuration, blind scrubbing, readback scrubbing, SEFI monitoring, reconfiguration in-orbit and UART interface communication functions. BSV5CBRH is SEU hardened and SEL immune.

3、 Packages and Pin Function Descriptions

3.1 Pin List

The pin list of BSV5CBRH is shown in table 3-1

Table 3-1 Pin List

Pin number	Pin name	Signal symbol	Direction	Function description
1	N13	Sysclk	I	System clock
2	N14	rst_n	I	System reset
3	M16	UART_BR_SEL[1]	I	UART Baud rate Selection
4	N15	UART_BR_SEL[0]	I	UART Baud rate Selection
5	M15	UART_IN	I	UART Interface Input
6	M14	UART_OUT	O	UART Interface Output
7	M13	UART_EN	O	UART Interface Output Enable
8	L13	UART_ID[4]	I	UART ID
9	L14	UART_ID[3]	I	UART ID
10	L15	UART_ID[2]	I	UART ID
11	L16	UART_ID[1]	I	UART ID
12	M12	UART_ID[0]	I	UART ID
13	K15	FLASH_WR	O	FLASH Write
14	K14	FLASH_OE	O	FLASH Output Enable
15	K13	FLASH_RESET	O	FLASH Reset
16	K16	FLASH_RY/BY	I	FLASH Ready/Busy
17	B5	FLASH_A[23]	O	FLASH Address
18	A5	FLASH_A[22]	O	FLASH Address
19	D5	FLASH_A[21]	O	FLASH Address
20	E14	FLASH_A[20]	O	FLASH Address
21	E13	FLASH_A[19]	O	FLASH Address
22	F16	FLASH_A[18]	O	FLASH Address
23	F15	FLASH_A[17]	O	FLASH Address
24	F14	FLASH_A[16]	O	FLASH Address
25	F13	FLASH_A[15]	O	FLASH Address
26	G16	FLASH_A[14]	O	FLASH Address
27	G15	FLASH_A[13]	O	FLASH Address
28	G14	FLASH_A[12]	O	FLASH Address
29	G13	FLASH_A[11]	O	FLASH Address
30	H16	FLASH_A[10]	O	FLASH Address
31	H15	FLASH_A[9]	O	FLASH Address
32	H14	FLASH_A[8]	O	FLASH Address
33	G12	FLASH_A[7]	O	FLASH Address

Pin number	Pin name	Signal symbol	Direction	Function description
34	H13	FLASH_A[6]	O	FLASH Address
35	J13	FLASH_A[5]	O	FLASH Address
36	H12	FLASH_A[4]	O	FLASH Address
37	J12	FLASH_A[3]	O	FLASH Address
38	J16	FLASH_A[2]	O	FLASH Address
39	J15	FLASH_A[1]	O	FLASH Address
40	J14	FLASH_A[0]	O	FLASH Address
41	A9	FLASH_D[15]	IO	FLASH Data
42	D9	FLASH_D[14]	IO	FLASH Data
43	C9	FLASH_D[13]	IO	FLASH Data
44	B9	FLASH_D[12]	IO	FLASH Data
45	B8	FLASH_D[11]	IO	FLASH Data
46	A8	FLASH_D[10]	IO	FLASH Data
47	D8	FLASH_D[9]	IO	FLASH Data
48	C8	FLASH_D[8]	IO	FLASH Data
49	C7	FLASH_D[7]	IO	FLASH Data
50	D7	FLASH_D[6]	IO	FLASH Data
51	A7	FLASH_D[5]	IO	FLASH Data
52	B7	FLASH_D[4]	IO	FLASH Data
53	B6	FLASH_D[3]	IO	FLASH Data
54	A6	FLASH_D[2]	IO	FLASH Data
55	C6	FLASH_D[1]	IO	FLASH Data
56	D6	FLASH_D[0]	IO	FLASH Data
57	G4	FPGA_M2	O	FPGA Mode
58	G2	FPGA_M1	O	FPGA Mode
59	G1	FPGA_M0	O	FPGA Mode
60	D10	SMAP_CCLK	O	SelectMAP Interface Clock
61	C12	SMAP_D[7]	IO	SelectMAP Interface Data
62	B11	SMAP_D[6]	IO	SelectMAP Interface Data
63	A11	SMAP_D[5]	IO	SelectMAP Interface Data
64	D11	SMAP_D[4]	IO	SelectMAP Interface Data
65	C11	SMAP_D[3]	IO	SelectMAP Interface Data
66	B10	SMAP_D[2]	IO	SelectMAP Interface Data
67	A10	SMAP_D[1]	IO	SelectMAP Interface Data
68	C10	SMAP_D[0]	IO	SelectMAP Interface Data
69	M1	FPGA_TCK	O	FPGA TCK
70	M2	PROM_CLK	O	PROM Clk
71	K1	PROM_D[7]	I	PROM Data
72	K2	PROM_D[6]	I	PROM Data
73	K4	PROM_D[5]	I	PROM Data

Pin number	Pin name	Signal symbol	Direction	Function description
74	K3	PROM_D[4]	I	PROM Data
75	L2	PROM_D[3]	I	PROM Data
76	L1	PROM_D[2]	I	PROM Data
77	L3	PROM_D[1]	I	PROM Data
78	L4	PROM_D[0]	I	PROM Data
79	J4	DYNA_PROG	I	FPGA Dynamic Configuration Enable
80	J3	MODE_SCRUB	I	FPGA Scrub Mode
81	J1	EN_SCRUB	I	FPGA Scrub Enable
82	H4	INTERVEL[2]	I	FPGA Scrubbing interval
83	H3	INTERVEL[1]	I	FPGA Scrubbing interval
84	J2	INTERVEL[0]	I	FPGA Scrubbing interval
85	H1	SEL_BIT	I	Bitstream Selection
86	H2	CON_EN_0	I	FPGA0 Control Enable
87	G3	PROG_B_0	O	FPGA0 Configuration Asynchronous Reset
88	F3	INIT_B_0	I	Connect to Initial pin of FPGA0
89	F4	DONE_0	I	Connect to Done pin of FPGA0
90	F1	BUSY_0	I	Connect to Busy pin of SelectMAP
91	F2	CS_B_0	O	Connect to CE pin of SelectMAP
92	E4	RDWR_B_0	O	Connect to RDWR Control pin of SelectMAP
93	E3	PROM_CE_0	O	Connect to CE pin of PROM0
94	T4	PROM_OE_0	O	Connect to OE pin of PROM0
95	P4	RESET_FPGA_0	O	FPGA0 Reset
96	R4	FLASH_CE_0	O	FLASH0 Chip Select
97	P5	CON_EN_1	I	FPGA1 Control Enable
98	R5	PROG_B_1	O	FPGA1 Configuration Asynchronous Reset
99	N4	INIT_B_1	I	Connect to Initial pin of FPGA1
100	N5	DONE_1	I	Connect to Done pin of FPGA1
101	T5	BUSY_1	I	Connect to Busy pin of SelectMAP
102	T6	CS_B_1	O	Connect to CE pin of SelectMAP
103	R6	RDWR_B_1	O	Connect to RDWR Control pin of SelectMAP
104	P6	PROM_CE_1	O	Connect to CE pin of PROM1

Pin number	Pin name	Signal symbol	Direction	Function description
105	N6	PROM_OE_1	O	Connect to OE pin of PROM1
106	T7	RESET_FPGA_1	O	FPGA1 Reset
107	R7	FLASH_CE_1	O	FLASH1 Chip Select
108	P7	CON_EN_2	I	FPGA2 Control Enable
109	N7	PROG_B_2	O	FPGA2 Configuration Asynchronous Reset
110	T8	INIT_B_2	I	Connect to Initial pin of FPGA2
111	R8	DONE_2	I	Connect to Done pin of FPGA2
112	P8	BUSY_2	I	Connect to Busy pin of SelectMAP
113	R9	CS_B_2	O	Connect to CE pin of SelectMAP
114	N8	RDWR_B_2	O	Connect to RDWR Control pin of SelectMAP
115	P9	PROM_CE_2	O	Connect to CE pin of PROM2
116	N9	PROM_OE_2	O	Connect to OE pin of PROM2
117	T9	RESET_FPGA_2	O	FPGA2 Reset
118	T10	FLASH_CE_2	O	FLASH2 Chip Select
119	R10	CON_EN_3	I	FPGA3 Control Enable
120	P10	PROG_B_3	O	FPGA3 Configuration Asynchronous Reset
121	N10	INIT_B_3	I	Connect to Initial pin of FPGA3
122	P12	DONE_3	I	Connect to Done pin of FPGA3
123	P11	BUSY_3	I	Connect to Busy pin of SelectMAP
124	N11	CS_B_3	O	Connect to CE pin of SelectMAP
125	N12	RDWR_B_3	O	Connect to RDWR Control pin of SelectMAP
126	R13	PROM_CE_3	O	Connect to CE pin of PROM3
127	R11	PROM_OE_3	O	Connect to OE pin of PROM3
128	R12	RESET_FPGA_3	O	FPGA3 Reset
129	T11	FLASH_CE_3	O	FLASH3 Chip Select
130	M4	DECODE_EN	I	Decode Enable
131	D13	BIST_RSTN	I	Test pin, Connect to GND
132	B12	BIST_EN	I	Test pin, Connect to GND
133	C13	BIST_CLK	I	Test pin, Connect to GND
134	A12	bist_mode	I	Test pin, Connect to GND
135	E2	scan_en	I	Test pin, Connect to GND
136	D3	scan_mode	I	Test pin, Connect to GND

Pin number	Pin name	Signal symbol	Direction	Function description
137	E11	VDD_VCCO33	P	IO Power Supply pin
138	G5	VDD_VCCINT18	P	Core power Supply
139	F12	VDD_VCCO33	P	IO Power Supply pin
140	H11	VDD_VCCO33	P	IO Power Supply pin
141	K5	VDD_VCCO33	P	IO Power Supply pin
142	E5	VDD_VCCO33	P	IO Power Supply pin
143	E8	VDD_VCCINT18	P	Core power Supply
144	E6	VDD_VCCO33	P	IO Power Supply pin
145	E7	VDD_VCCO33	P	IO Power Supply pin
146	E9	VDD_VCCINT18	P	Core power Supply
147	E10	VDD_VCCO33	P	IO Power Supply pin
148	J11	VDD_VCCINT18	P	Core power Supply
149	F11	VDD_VCCO33	P	IO Power Supply pin
150	E12	VDD_VCCO33	P	IO Power Supply pin
151	F5	VDD_VCCO33	P	IO Power Supply pin
152	H5	VDD_VCCINT18	P	Core power Supply
153	L5	VDD_VCCO33	P	IO Power Supply pin
154	K11	VDD_VCCINT18	P	Kernel power Supply
155	L6	VDD_VCCO33	P	IO Power Supply pin
156	L11	VDD_VCCO33	P	IO Power Supply pin
157	M5	VDD_VCCO33	P	IO Power Supply pin
158	J5	VDD_VCCINT18	P	Core power Supply
159	F6	VDD_VCCO33	P	IO Power Supply pin
160	M9	VDD_VCCO33	P	IO Power Supply pin
161	M6	VDD_VCCINT18	P	Core power Supply
162	M10	VDD_VCCO33	P	IO Power Supply pin
163	M11	VDD_VCCO33	P	IO Power Supply pin
164	M7	VDD_VCCINT18	P	Core power Supply
165	M8	VDD_VCCINT18	P	Core power Supply
166	F9	GND	P	GND pin
167	F10	GND	P	GND pin
168	G6	GND	P	GND pin
169	K8	GND	P	GND pin
170	K9	GND	P	GND pin
171	F7	GND	P	GND pin
172	F8	GND	P	GND pin
173	J7	GND	P	GND pin
174	J8	GND	P	GND pin
175	J9	GND	P	GND pin
176	J10	GND	P	GND pin

Pin number	Pin name	Signal symbol	Direction	Function description
177	K6	GND	P	GND pin
178	K7	GND	P	GND pin
179	G7	GND	P	GND pin
180	G8	GND	P	GND pin
181	G9	GND	P	GND pin
182	G10	GND	P	GND pin
183	G11	GND	P	GND pin
184	K10	GND	P	GND pin
185	L7	GND	P	GND pin
186	L8	GND	P	GND pin
187	H6	GND	P	GND pin
188	H7	GND	P	GND pin
189	H8	GND	P	GND pin
190	H9	GND	P	GND pin
191	H10	GND	P	GND pin
192	J6	GND	P	GND pin
193	L9	GND	P	GND pin
194	L10	GND	P	GND pin
195	A1	NC	-	-
196	A13	NC	-	-
197	A14	NC	-	-
198	A15	NC	-	-
199	A16	NC	-	-
200	A2	NC	-	-
201	A3	NC	-	-
202	A4	NC	-	-
203	B1	NC	-	-
204	B13	NC	-	-
205	B14	NC	-	-
206	B15	NC	-	-
207	B16	NC	-	-
208	B2	NC	-	-
209	B3	NC	-	-
210	B4	NC	-	-
211	C1	NC	-	-
212	C14	NC	-	-
213	C15	NC	-	-
214	C16	NC	-	-
215	C2	NC	-	-
216	C3	NC	-	-

Pin number	Pin name	Signal symbol	Direction	Function description
217	C4	NC	-	-
218	C5	NC	-	-
219	D1	NC	-	-
220	D14	NC	-	-
221	D15	NC	-	-
222	D16	NC	-	-
223	D2	NC	-	-
224	D4	NC	-	-
225	E15	NC	-	-
226	E16	NC	-	-
227	K12	NC	-	-
228	L12	NC	-	-
229	M3	NC	-	-
230	N1	NC	-	-
231	N16	NC	-	-
232	N2	NC	-	-
233	N3	NC	-	-
234	P1	NC	-	-
235	P13	NC	-	-
236	P14	NC	-	-
237	P15	NC	-	-
238	P16	NC	-	-
239	P2	NC	-	-
240	P3	NC	-	-
241	R1	NC	-	-
242	R14	NC	-	-
243	R15	NC	-	-
244	R16	NC	-	-
245	R2	NC	-	-
246	R3	NC	-	-
247	T1	NC	-	-
248	T12	NC	-	-
249	T13	NC	-	-
250	T14	NC	-	-
251	T15	NC	-	-
252	T16	NC	-	-
253	T2	NC	-	-
254	T3	NC	-	-
255	D12	Reserved_1	-	Reservations port. Internal pull up, Floating or power supply is

Pin number	Pin name	Signal symbol	Direction	Function description
				recommended
256	E1	Reserved_2	-	Reservations port. Internal pull down, Floating or grounding is recommended

3.2 Pin Function Description

Table 3-2 Pin Function Description

Pin symbol	Direction	Pin State	Function
Sysclk	I	Pull up	System clock. All functions are driven by the clock. Maximum Working Frequency: 20MHz. And the continuous clock is recommended.
rst_n	I	Pull up	System reset signal. Active low.
UART_BR_SEL[1:0]	I	Pull down	UART Baud rate setting signal. “00”: 1280000bps, “01”: 628000bps, “10”: 115200bps, “11”: 57600bps.
UART_IN	I	Pull up	UART Interface Input
UART_OUT	O	Pull up	UART Interface Output
UART_EN	O	Pull down	UART Interface Output Enable signal. Active high.
UART_ID[4:0]	I	Pull up	UART ID
FLASH_WR	O	Pull up	FLASH Write signal. Active low, high level is invalid.
FLASH_OE	O	Pull up	FLASH Output Enable signal. Low level indicates output disable and high level indicates output enable.
FLASH_RESET	O	Pull up	FLASH Reset signal, active low.
FLASH_RY/BY	I	Pull up	FLASH Ready/Busy signal.
FLASH_A[23:0]	O	Pull up	FLASH Address
FLASH_D[15:0]	IO	Pull up	FLASH Data
FPGA_M2	O	Pull up	FPGA mode selection
FPGA_M1	O	Pull up	
FPGA_M0	O	Pull down	
SMAP_CCLK	O	Pull up	SelectMAP Interface Clock signal

SMAP_D[7:0]	IO	Pull up	SelectMAP Interface data signal
FPGA_TCK	O	Pull up	FPGA TCK
PROM_CLK	O	Pull up	Connect to clk pin of PROM
PROM_D [7:0]	I	Pull up	Connect to data pin of PROM
DYNA_PROG	I	Pull up	FPGA Dynamic Configuration Enable signal. 0: disable, 1: enable.
MODE_SCRUB	I	Pull up	FPGA Scrubbing Mode signal. 0: blind scrubbing, 1: readback scrubbing.
EN_SCRUB	I	Pull up	FPGA Scrub Enable signal. 0: Scrubbing disable, 1: Scrubbing enable.
INTERVEL[2:0]	I	Pull down	FPGA Scrubbing/Readback interval signal. 8 options ranging from ‘’000’’ to “111”.
SEL_BIT	I	Pull up	FPGA bitstream selection signal. 0: from PROM 1: from FLASH
CON_EN_0	I	Pull up	FPGA0 Control Enable signal. 1: enable, 0: disable.
PROG_B_0	O	Pull up	FPGA0 Configuration Asynchronous Reset. Active low.
INIT_B_0	I	Pull up	Connect to Initial pin of FPGA0. 0: Initializing or CRC false, 1: Initialized or CRC true.
DONE_0	I	Pull up	Connect to Done pin of FPGA0. 0: fail, 1: succeed.
BUSY_0	I	Pull down	Connect to Busy pin of SelectMAP.
CS_B_0	O	Pull up	Connect to CE pin of SelectMAP .
RDWR_B_0	O	Pull up	Connect to RDWR Control pin of SelectMAP .
PROM_CE_0	O	Pull up	Connect to CE pin of PROM0.
PROM_OE_0	O	Pull up	Connect to OE pin of PROM0.
RESET_FPGA_0	O	Pull up	FPGA0 Reset signal. After power-on configuration is successful, BSV5CBRH sends the resetting signal to FPGA. Active low.
FLASH_CE_0	O	Pull up	FLASH0 Chip Select
CON_EN_1	I	Pull up	FPGA1 Control Enable signal. 1: enable, 0: disable.

PROG_B_1	O	Pull up	FPGA1 Configuration Asynchronous Reset. Active low.
INIT_B_1	I	Pull up	Connect to Initial pin of FPGA1. 0: Initializing or CRC false, 1: Initialized or CRC true.
DONE_1	I	Pull up	Connect to Done pin of FPGA1. 0: Fail, 1: succeeded.
BUSY_1	I	Pull down	Connect to Busy pin of SelectMAP.
CS_B_1	O	Pull up	Connect to CE pin of SelectMAP .
RDWR_B_1	O	Pull up	Connect to RDWR Control pin of SelectMAP .
PROM_CE_1	O	Pull up	Connect to CE pin of PROM1.
PROM_OE_1	O	Pull up	Connect to OE pin of PROM1.
RESET_FPGA_1	O	pull up	FPGA1 Reset signal. After power-on configuration is successful, BSV5CBRH sends the resetting signal to FPGA. Active low.
FLASH_CE_1	O	Pull up	FLASH1 Chip Select (subarea: 1).
CON_EN_2	I	Pull up	FPGA2 Control Enable signal. 1: enable, 0: disable.
PROG_B_2	O	Pull up	FPGA2 Configuration Asynchronous Reset. Active low.
INIT_B_2	I	Pull up	Connect to Initial pin of FPGA2. 0: Initializing or CRC false, 1: Initialized or CRC true.
DONE_2	I	Pull up	Connect to Done pin of FPGA2. 0: fail, 1: succeed.
BUSY_2	I	Pull down	Connect to Busy pin of SelectMAP.
CS_B_2	O	Pull up	Connect to CE pin of SelectMAP .
RDWR_B_2	O	Pull up	Connect to RDWR Control pin of SelectMAP .
PROM_CE_2	O	Pull up	Connect to CE pin of PROM2.
PROM_OE_2	O	Pull up	Connect to OE pin of PROM2. 0: output is enable, 1: output is disable.
RESET_FPGA_2	O	Pull up	FPGA2 Reset signal. After power-on configuration is successful, BSV5CBRH sends the resetting signal to FPGA. Active low.
FLASH_CE_2	O	Pull up	FLASH2 Chip Select (subarea: 2).

CON_EN_3	I	Pull up	FPGA3 Control Enable signal. 1: enable, 0: disable.
PROG_B_3	O	Pull up	FPGA3 Configuration Asynchronous Reset. Active low.
INIT_B_3	I	Pull up	Connect to Initial pin of FPGA3. 0: Initializing or CRC false, 1: Initialized or CRC true.
DONE_3	I	Pull up	Connect to Done pin of FPGA3. 0: fail, 1: succeed.
BUSY_3	I	Pull down	Connect to Busy pin of SelectMAP.
CS_B_3	O	Pull up	Connect to CE pin of SelectMAP .
RDWR_B_3	O	Pull up	Connect to RDWR Control pin of SelectMAP .
PROM_CE_3	O	Pull up	Connect to CE pin of PROM3.
PROM_OE_3	O	Pull up	Connect to OE pin of PROM3.
RESET_FPGA_3	O	Pull up	FPGA3 Reset signal. After power-on configuration is successful, BSV5CBRH sends the resetting signal to FPGA. Active low.
FLASH_CE_3	O	Pull up	FLASH3 Chip Select.
DECODE_EN	I	Pull down	Decode Enable signal. When the FLASH stores the BCH bit stream, this signal can control the decoding operation. 0: Decode, 1: Don’t decode, Default: low level.

3.3 Package

The CBGA256 package is shown in figure 3-1。

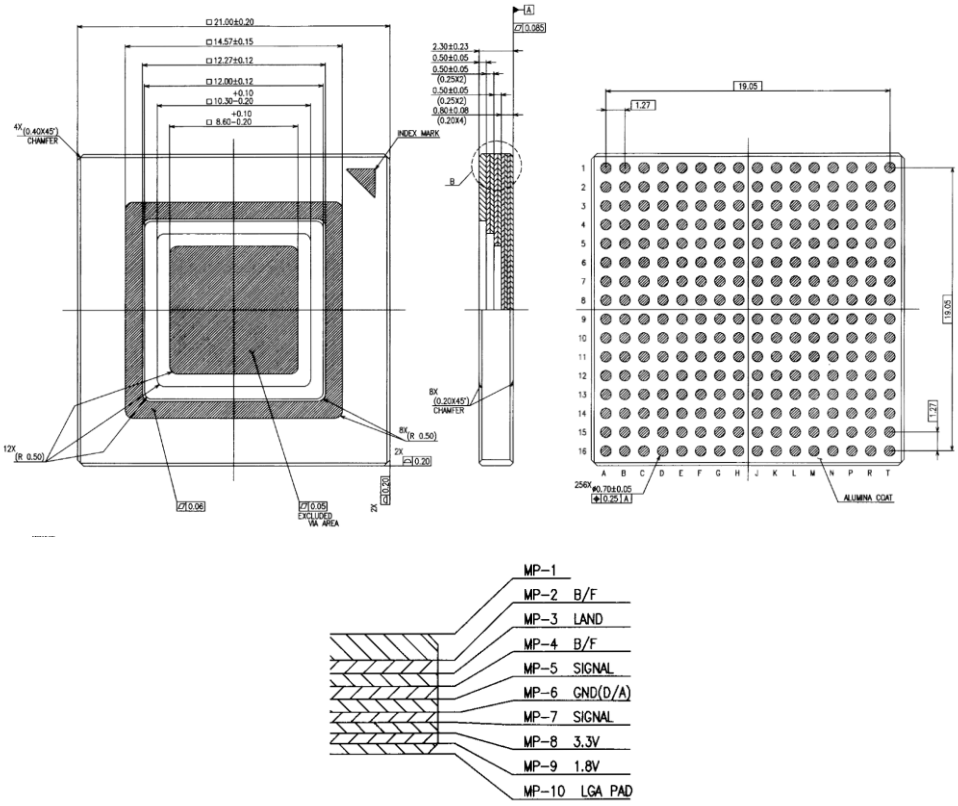


Figure 3-1 CBGA256 package

4、 Functionality Description

BSV5CBRH is classified as aerospace grade product which provides an integrated solution including power-on/reset configuration, blind scrubbing, readback scrubbing and SEFI monitor to mitigate single event upset(SEU) happened in space application SRAM FPGAs. The BSV5CBRH chip significantly reduces the degree of difficulty and complexity in designing scrubbing system.

4.1 Function block diagram

BSV5CBRH function block diagram is shown in figure 4-1.

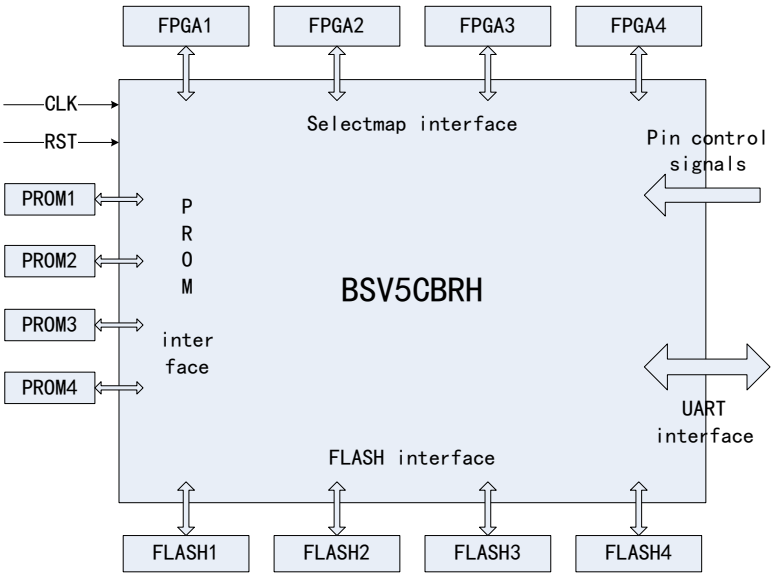


Figure 4-1 BSV5CBRH function block diagram

Figure 4-1 shows the peripheral devices, including under-scrubbing FPGAs, PROM chips for bitstream storage, FLASH chips for bitstream uploading, 20MHz Oscillators, etc. The corresponding external interfaces are system clock, asynchronous reset, SelectMAP interface, PROM interface, FLASH interface, Pin control signals and UART interface.

4.2 Product function description

BSV5CBRH mainly works in FPGA configuration, FPGA scrubbing and FPGA readback patterns. It's capable of communicating with MCU/CPU through UART interface. Operations like FLASH erase and program is also carried out through UART.

The main functions of BSV5CBRH are as follows:

4.2.1 FPGA configuration

Configuration function indicates basic Power-on /reset configuration and several Reconfiguration operations. It writes data in FPGA configuration memory and makes FPGA run in an expected function. The BSV5CBRH internal status registers could tell information about FPGA's operation state.

(1) Power-on/reset Configuration: BSV5CBRH reads the configuration data from PROM/FLASH and puts the data on FPGA SelectMAP data pins straight away. FPGA should be in slave parallel mode. The time spent to configure FPGA through

BSV5CBRH is the same as to configure FPGA directly with PROM/FLASH.

(2) Dynamical Reconfiguration: Pin-control signals or instructions from UART interface set the dynamical reconfiguration enable/disable option. Default setting depends on voltage level on the dedicated control pins. When the enable option is on, BSV5CBRH will reconfigure FPGA if a SEFI happened.

(3) Instruction Reconfiguration: BSV5CBRH receives instruction from other controller through UART interface to reconfigure FPGA.

4.2.2 FPGA scrubbing

To repair SEU errors in the SRAM FPGA configuration memory, BSV5CBRH rewrites data stored in the configuration memory array via SelectMAP interface without disrupting its operations, which is called scrubbing. The detailed descriptions are as follows:

(1) Scrubbing Enable/Disable: BSV5CBRH sets scrubbing enable/disable option according to pin level or UART instruction.

(2) Blind scrubbing: BSV5CBRH reads configuration data from bitstream storage devices and rewrite it into the accessible district of FPGA configuration memory array periodically. The period of blind scrubbing is set by dedicated pin or UART instruction. (Scrubbing period indicates the time interval between the end of current scrubbing operation and the start of next operation.)

(3) Readback scrubbing: Readback CRC is performed periodically to detect SEU. The CRC which is different from the GoldenCRC will be considered as a SEU error and trigger a scrubbing operation. The setting of Readback CRC period is the same as blind scrubbing.

4.2.3 FPGA readback

Readback check: BSV5CBRH periodically readbacks configuration data and calculates a CRC value. The value is saved in internal status register (ADDR 0x04) and refreshed in every round of readback. The setting of readback check period is the same as blind scrubbing. And the period indicates the time interval between the end of current readback operation and the start of next operation.

Readback CRC: After power-on/reset configuration is done, the first round of Readback CRC generates a CRC value as golden value for later comparison. If BSV5CBRH works in the pattern of readback scrubbing, the subsequent readback

CRC value are compared against the golden value. When a CRC mismatch is found, the SEU error flag is asserted and the error status is updated in register (ADDR 0x06).

4.2.4 FPGA SEFI monitor

Both FPGA operating status and BSV5CBRH internal register value are monitored to determine when a SEFI happened and perform a recovery operation. A combination of different detection methods of DONE pin, BUSY pin, FAR register and STATUS register is implemented to identify SEFIs. When a SEFI is asserted, the error status will be updated in BSV5CBRH internal register (ADDR 0x05) and BSV5CBRH will reconfigure the FPGA immediately when the dynamically reconfiguration enable option is on.

4.2.5 UART communication

The UART interface enables BSV5CBRH to communicate with other controller, implementing instruction transmitting and register values capturing. Work pattern setting and status monitoring can be done through UART.

4.3 Scrubbing cycle

Scrubbing cycles is related to the size of bitstream and clock frequency. The calculation formula is:

T= size of bitstream × clock period

The typical scrubbing cycles are shown in table 4-1.

Table 4-1 BSV5CBRH scrubbing cycles

Device	Size of scrubbing data (bytes)	Clock frequency	Scrubbing cycle
XQVR300	207,900	10MHz	About 20.8 ms
XQR2V3000	944,208	10MHz	About 94.4 ms
XQR5VSX95T	3,117,476	10MHz	About 311.8 ms
XQR5VLX155T	4,201,188	10MHz	About 420.2 ms
XQR5VFX130T	4,260,884	10MHz	About 426 ms

5、 Storage Condition

Packaged product should be stored in the ventilate warehouse with ambient

temperature 10℃～30℃ and relative humidity less than 70%. There should be no acid, alkali or other radiant gas in the environment.

6、 Absolute Maximum Ratings

a) Pin Supply voltage range to ground potential（V_{CCO}）： -0.3 V ～4.0 V
b) Core Supply voltage range to ground potential（V_{CCINT}）： -0.3 V ～2.0 V
c) DC input voltage range（V_{IN}）： -0.3 V ～4.7 V
d) Storage temperature（T_{stg}）： -65 ℃～ 150 ℃
e) Lead temperature（T_{SOL}）： 220 ℃
f) Thermal resistance（$R_{th(J-C)}$）： 2.945 ℃/W
g) Power dissipation（P_D）： 0.5 W

7、 Recommended Operation Conditions

a) Pin Supply voltage relative to ground（V_{CCO}）： 3.3 ±10%V
b) Core Supply voltage relative to ground（V_{CCINT}）： 1.8 ±10%V
c) Case operation temperature range(T_A) ： -55℃~+125℃
d) Operation frequency（f）： 20MHz

8、 Specifications

All electrical characteristics are shown in table 8-1.

Table 8-1 BSV5CBRH electrical characteristics

Test	Symbol	Conditions（V_{CCO}=3.3V±10%，V_{CCINT}=1.8V±10%，-55℃≤T_A≤125℃）	Limits		units
			min	max	
Output high voltage	V_{OH}	V_{CCO}=2.97V，I_{OH}=-4 mA，test all output/bidirectional ports	2.7	—	V
Output low voltage	V_{OL}	V_{CCO}=2.97V，I_{OL}=4mA。，test all output/bidirectional ports	—	0.3	V
Input high voltage	V_{IH}	V_{CCO}=2.97V, V_{CCINT}=1.62V, test all input ports	2.0	—	V
Input low voltage	V_{IL}	V_{CCO}=2.97V, V_{CCINT}=1.62V, test all input ports	—	0.7	V
Pad pull up leakage current	I_{RPU}	V_{IN}=0V，V_{CCO}=3.63V	-150	—	μA
Pad pull down leakage current	I_{RPD}	V_{IN}=V_{CCO}，V_{CCO}=3.63V	—	150	μA
Quiescent core supply	I_{CCINTQ}	V_{CCINT}=1.98V,	—	400	μA

current		V_{CCO}=3.63V			
Quiescent pin supply current	I_{CCOQ}	V_{CCINT}=1.98V, V_{CCO}=3.63V	—	40	μA
Dynamical core supply current	I_{CCINTD}	f=20MHz,V_{CCO}=3.63V, V_{CCINT}=1.98V, test V_{CCINT} ports with open output	—	200	mA
Dynamical pin supply current	I_{CCOD}	f=20MHz,V_{CCO}=3.63V, V_{CCINT}=1.98V,test V_{CCO} ports with open output	—	100	mA
Input capacitance	C_{IN}	f=1MHz， V_{CCO}=0V, V_{CCINT}=0V,T_A=25℃	—	12	pF
Function test	—	f=20MHz	—	—	—
Output delay: SMAP_D0 relative to SMAP_CCLK	T_{c2d_d0}	V_{CCO}=2.97V, V_{CCINT}=1.62V, f=20MHz	—	40	ns
Output delay: SMAP_D1 relative to SMAP_CCLK	T_{c2d_d1}		—	40	ns
Output delay: SMAP_D2 relative to SMAP_CCLK	T_{c2d_d2}		—	40	ns
Output delay: SMAP_D3 relative to SMAP_CCLK	T_{c2d_d3}		—	40	ns
Output delay: SMAP_D4 relative to SMAP_CCLK	T_{c2d_d4}			40	ns
Output delay: SMAP_D5 relative to SMAP_CCLK	T_{c2d_d5}			40	ns
Output delay: SMAP_D6 relative to SMAP_CCLK	T_{c2d_d6}			40	ns
Output delay: SMAP_D7 relative to SMAP_CCLK	T_{c2d_d7}			40	ns

9、 Package Specifications

The specifications of CBGA256 package are shown in figure 9-1.

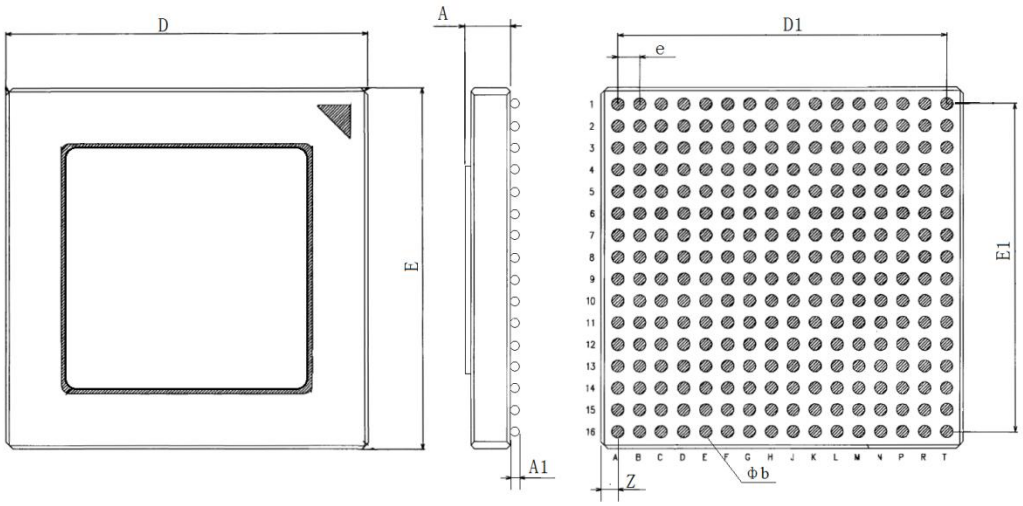


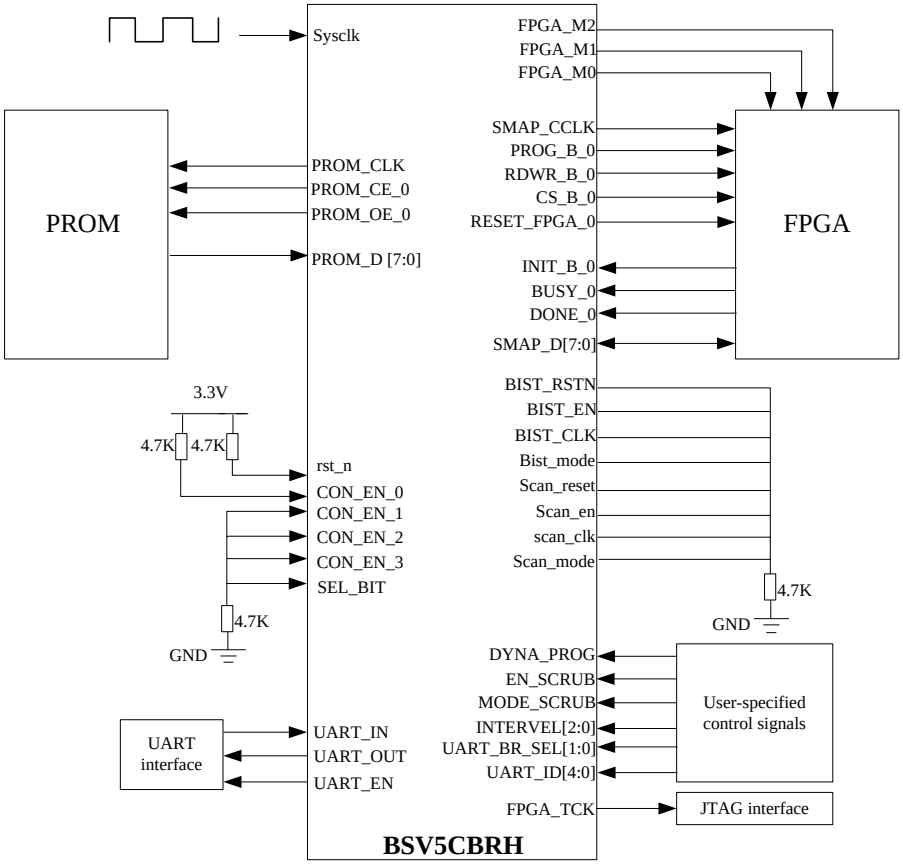
Figure 9-1 CBGA256 package specifications

Table 9-1 size symbol list

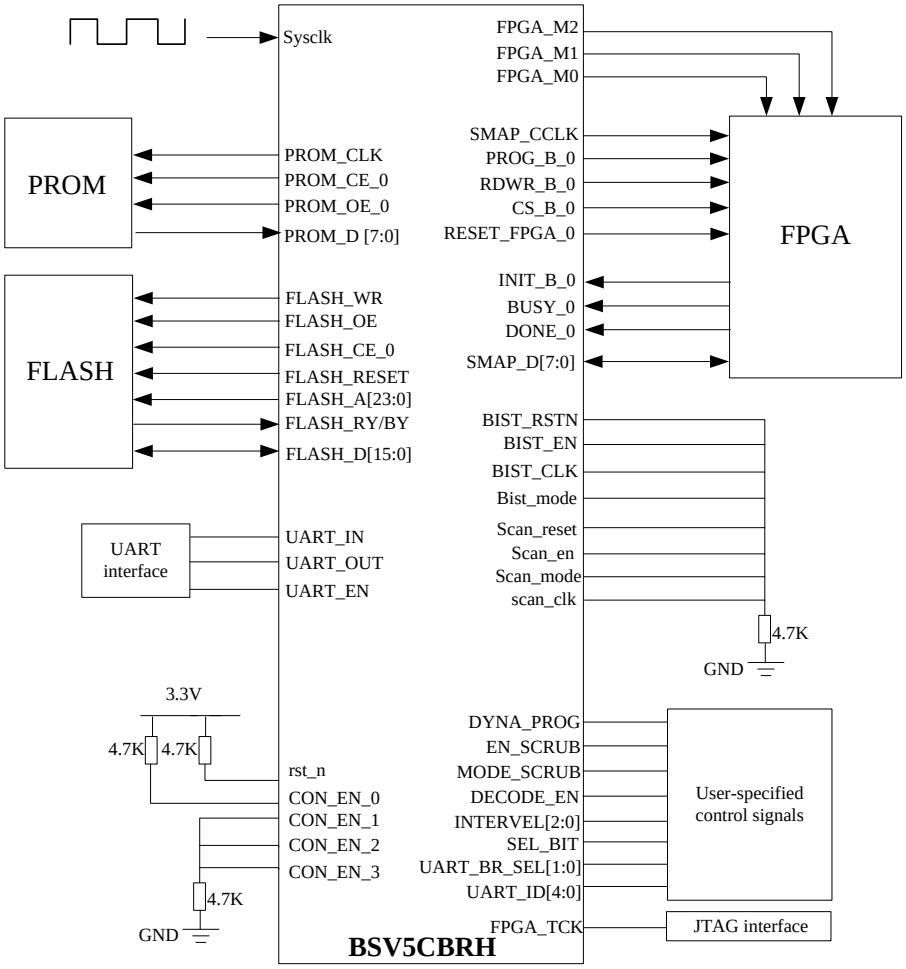
Size symbol	Value（unit：mm）		
	min	typical	max
A	2.00	—	3.00
A1	0.72	—	0.90
D	20.50	—	21.50
E	20.50	—	21.50
D1	18.75	—	19.35
E1	18.75	—	19.35
e	—	1.27	—
ϕb	0.60	—	0.80
Z	0.50	—	1.20

10、 Appendix I Typical Application Example

BSV5CBRH is placed between FPGA and PROM/FLASH working as a data Exchange Bridge. It configures and scrubs FPGA in slave parallel mode. Two application examples of scrubbing one FPGA chip with PROM and scrubbing one FPGA chip with both PROM and FLASH are respectively shown in figure 1-1 and figure 1-2, where the FPGA pins program and initial are pulled up with 4.7KΩ resistance, done pin is pulled up with 330Ω resistance. The CCLK source is BSV5CBRH.



Appendix Figure 1-1 Typical Application Example 1: one scrubbed FPGA with PROM



Appendix Figure 1-2 Typical Application Example 2: one scrubbed FPGA with PROM and FLASH

Attentions：

- Configuration bit stream and the PROM mcs format file should be generated by a Xilinx software.
- Keep the default size of bit stream; do not use any options that could change the default size, such as bit compression.
- Do not use disable readback option or disable reconfiguration option in ISE.
- Do not use LUT-RAM or LUT-shifter

Service and Support：

Address：No.2 Siyingmen North Road, Donggaodi, Fengtai District, Beijing, China
Department：Department of international cooperation
Telephone：010-68757343
Fax：010-68757706
Zip code：100076